

<b>FORM PTO-1449</b> U.S. Department of Commerce (Rev. 4/92) Patent and Trademark Office	<b>ATTY. DOCKET NO.</b>	<b>SERIAL NO.</b>
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	<b>500.28166CX2</b>	<b>N t y t assigned</b>
(Use several sheets if necessary)	<b>APPLICANT</b> <b>HOTTA, et al</b>	
	<b>FILING DATE</b> <b>May 14, 2001</b>	<b>GROUP</b> <b>2152</b>

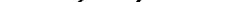
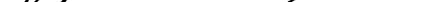
## U.S. PATENT DOCUMENTS

## FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER							DATE	COUNTRY	CLASS	SUBCLASS	ABSTRACT		
													YES	NO	
1		0	1	4	9	0	4	9	7/85	EPO					
2		0	2	6	0	4	0	9	3/88	EPO					
3		8	8	0	9	0	3	5	11/88	WIPO					
4		0	0	8	2	9	0	3	7/83	EPO					
5		6	3	7	3	3	3	2	2/88	Japan					XX

**OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)**

<i>[Signature]</i>	Technical Summary, Multi-flow Computer, Inc., 4/30/87, pp/ 1-(3-7).
<i>[Signature]</i>	O. Serlin, "The Serlin Report on Parallel Processing", ITOM International Co., Issue No. 7, 12/87, pp. 10-18.
<i>[Signature]</i>	IEEE Journal of Solid-State Circuits, "MIPS-X: A 20-MIPS Peak 32-Bit Microprocessor with on-chip Cache", Horowitz, et al, vol. sc-22, No. 5, October 1987, New York.
<i>[Signature]</i>	J. Bond, "Parallel Processing Concepts Finally come together in Real Systems", Computer Design, June 1, 1987, pp. 51-74.

**EXAMINER**  **DATE CONSIDERED** 

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<i>u</i>		4	5	9	2	3	2		12/91	EPO					
<i>u</i>		3	2	8	8	2	4	6	12/91	Japan					XX
<i>u</i>		4	5	5	9	6	6		11/91	EPO					
<i>u</i>		6	3	1	3	1	2	3	0	6/88	Japan				

**OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)**

<i>g</i>	R. Acosta, et al, "An Instruction Issuing Approach to Enhancing Performance in Multiple Functional Unit Processors", IEEE Transactions on Computers vol. C-35, No. 9, Sept. 1986, pp. 815-828.
<i>h</i>	D. Ditzel, et al "The Hardware Architecture of the Crisp Microprocessor" ACM, 0084-7495, pp. 309-319.
<i>h</i>	Capozzi et al, "Non-sequential High-performance Processing", IBM Technical Disclosure Bulletin, vol. 27, No. 5, 10/84, pp. 2842-2844.

**EXAMINER:** Initial if citation is considered, draw line through citation if not in conformance and not considered.

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								May 14, 2001	2152	

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09/05/1999  
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EXAMINER INITIAL	DOCUMENT NUMBER								DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
h	4	9	4	2	5	2	5	7/90	Shintani et al	395	Dig. 1	11/20/87	
a	5	2	8	7	4	6	5	2/94	Kurosawa et al				
z	5	4	0	4	4	7	2	4/95	Kurosawa et al				
z	5	5	6	1	7	7	5	10/96	Kurosawa et al				
a	4	4	7	6	5	2	5	10/84	Ishii	364	Dig. 1		
a	4	5	9	4	6	5	5	6/86	Hdo et al	364	DIG. 1		
z	4	6	2	6	9	8	9	12/86	Rorii	395	375		
z	4	6	4	4	4	6	6	2/87	Saito	395	725		
a	4	7	9	4	5	1	7	12/88	Jones et al	395	725		
h	4	9	1	6	6	0	6	4/90	Yamaoka et al	395	375		
w	4	9	2	8	2	2	3	5/90	Dao et al	395	375		

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		DOCUMENT NUMBER								DATE	COUNTRY	CLASS	SUBCLASS	ABSTRACT		
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z	z	0	1	4	7	8	5	8	7/85	EPO						
z	z	0	0	4	2	4	4	2	12/81	EPO						
z	z	0	2	3	9	0	8	1	9/87	EPO						
z	z	0	1	0	1	5	9	6	8/83	EPO						

### OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

z	J. David, "Reducing the Branch Penalty in Pipelined Processors", Computer (July 1988), pp. 47-55.
z	Miller et al "Floating-Duplex Decode and Execution of Instruction", IBM Technical Disclosure Bulletin, vol. 23, No. 1, June 1980, pp. 409-412.
z	G. Tjoden et al, "Detection and Parallel Execution of Independent Instructions", IEEE Transaction, vol. C-19, No. 10, October 1970, pp. 889-895.

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